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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,752	10/18/2005	Masaru Wasaki	125703	5971

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EXAMINER	
HAM, SEUNGSOOK	
ART UNIT	**PAPER NUMBER**
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,752	WASAKI ET AL.	
	Examiner	Art Unit	
	Seungsook Ham	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 4, “creates a potential difference” cannot be understood as what is mean by "potential difference" (e.g., phase difference?).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by JP 57-8247.

JP 57-8247 (figs. 4 and 5) discloses a normal mode noise suppressing circuit comprising: at least one noise suppressing section (3, 4, 6) for suppressing normal mode noise disposed between two capacitors 8; the at least one noise suppressing section incorporates: a first detection/injection section having a first inductance 3 inserted to a first conductor line (the conductor line where input terminal 1 is connected to) at a specific first point, and a second inductance element 4 coupled to the first inductance element; a injection signal transmission path includes a capacitor 6 for detection and injection that allows the injection signal to pass (see fig. 1, I_1 and I_2); the injection signal transmission path has an end connected to the first conductor line at a second point different from the first point and the other end connected to the second conductor line 1'; the second inductance element 4 is inserted somewhere along the injection signal transmission path; and a node between the injection signal transmission path and the first conductor line forms a second detection/injection section (the node that is connected to the capacitor 6 and the conductor line connected to the terminal 1). It should be noted that the limitation recited in claim 1, lines 20-26 is inherent from the device of JP 57-8247 since the signal can be pass through either terminal 1, 1' or terminal 2, 2'.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP 57-8247 in view of Imamura et al. (JP 02-206360).

JP 57-8247 does not show providing third and fourth inductance elements, and the second and fourth inductance elements are inserted in series.

Imamura et al. (fig. 1) discloses a noise suppressing circuit having first and second inductance elements coupled to each other 37A, 37B, third and fourth inductance elements coupled to each other 38, 38 B, and the second and fourth inductance elements 37B, 38B are in series and a capacitor 40 is inserted along the injection signal transmission path. It should be noted that the noise suppressing circuit 30 is functionally equivalent to the noise suppressing section (3, 4, 6) in JP 57-8247.

It would have been obvious to one of ordinary skill in the art to provide the noise suppressing circuit of Imamura et al. as the noise suppressing section in the device of JP 57-8247 since both circuits are functionally equivalent and also provide a balanced signals in two conductor lines as shown by Imamura et al.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 57-8247 in view of Okochi et al. (US '362).

JP 57-8247 does not show providing two noise suppressing sections.

Okochi et al. (figs. 1-9, 11 and 12) discloses a filter having two stage noise suppressing sections L1& L2 (fig. 2), LLa& LLb (fig. 1), LA&LB (figs. 8 and 9) and teaches two stage type noise suppressing circuit advantage over single stage type noise suppressing circuit to attenuate a normal mode noise (col. 6, lines 14-29).

Therefore, it would have been obvious to one of ordinary skill in the art to provide a second noise suppressing circuit coupled to the capacitor 8 in the device of JP 57-8247 to improve the suppression of a normal mode noise as taught by Okochi et al.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-6 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 7-13 of U.S. Patent No. 7,256,662 in view of Okochi et al. (US '362).

The instant claims are the same except providing at least one capacitor coupled to the at least one noise suppressing section. However, providing a capacitor coupled to a noise suppressing section to suppress a normal mode is well known in the art. Okochi et al. (fig. 1) shows a noise suppressing circuit having at least one capacitor Cxo, Cx1, Cx2 for normal mode suppression. Thus, it would have been obvious to provide at least one capacitor coupled to the noise suppression section of the patent claims to attenuate/suppress a normal mode noise as shown by Okochi et al.

Moreover, providing a second noise suppression section is considered as an obvious design modification since Okochi et al. (figs. 1-9, 11 and 12) also teaches that two stage type noise suppression circuit is advantage over a single stage type noise suppression circuit to suppress a normal mode noise (see Okochi et al., col. 17-30).

Claims 7 and 8 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 7-13 of U.S. Patent No. 7,256,662 in view of Okochi et al. (US '362) and Imamura et al. (JP 02-206360).

The modified device of the patent claims lacks providing third and fourth inductance elements.

Imamura et al. (fig. 1) discloses a noise suppressing circuit having first and second inductance elements coupled to each other 37A, 37B, third and fourth inductance elements coupled to each other 38, 38 B, and the second and fourth

inductance elements 37B, 38B are in series and a capacitor 40 is inserted along the injection signal transmission path. It should be noted that the noise suppressing circuit 30 is functionally equivalent to the noise suppressing section in the patent claims. Moreover, Okochi et al. (figs. 1-2) discloses an inductance element in a second conductor line to provide a balanced signal.

Therefore, it would have been obvious to one of ordinary skill in the art to provide the noise suppressing circuit of Imamura et al. as the noise suppressing section in the modified device of patent claims since both circuits are functionally equivalent and also provide a balanced signals in two conductor lines as shown by Imamura et al.

Claims 1-6 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-12 of copending Application No. 10/557,995 in view of Okochi et al. (US '362).

The instant claims are the same except providing at least one capacitor coupled to the at least one noise suppressing section. However, providing a capacitor coupled to a noise suppressing section to suppress a normal mode is well known in the art. Okochi et al. (fig. 1) shows a noise suppressing circuit having at least one capacitor Cxo, Cx1, Cx2 for normal mode suppression. Thus, it would have been obvious to provide at least one capacitor coupled to the noise suppression section of the patent claims to attenuate/suppress a normal mode noise as shown by Okochi et al.

Moreover, providing a second noise suppression section is considered as an obvious design modification since Okochi et al. (figs. 1-9, 11 and 12) also teaches that

two stage type noise suppression circuit is advantage over a single stage type noise suppression circuit to suppress a normal mode noise (see Okochi et al., col. 17-30).

This is a provisional obviousness-type double patenting rejection.

Claims 7 and 8 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-12 of copending Application No. 10/557,995 in view of Okochi et al. (US '362) and Imamura et al. (JP 02-206360).

The modified device of the patent claims lacks providing third and fourth inductance elements.

Imamura et al. (fig. 1) discloses a noise suppressing circuit having first and second inductance elements coupled to each other 37A, 37B, third and fourth inductance elements coupled to each other 38, 38 B, and the second and fourth inductance elements 37B, 38B are in series and a capacitor 40 is inserted along the injection signal transmission path. It should be noted that the noise suppressing circuit 30 is functionally equivalent to the noise suppressing section in the patent claims. Moreover, Okochi et al. (figs. 1-2) discloses an inductance element in a second conductor line to provide a balanced signal.

Therefore, it would have been obvious to one of ordinary skill in the art to provide the noise suppressing circuit of Imamura et al. as the noise suppressing section in the modified device of patent claims since both circuits are functionally equivalent and also provide a balanced signals in two conductor lines as shown by Imamura et al.

This is a provisional obviousness-type double patenting rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Neuman and Wang et al. disclose a noise suppressing circuit having a cascade noise suppression sections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seungsook Ham whose telephone number is (571) 272-2405. The examiner can normally be reached on Monday-Thursday, 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571)-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Seungsook Ham
Primary Examiner
Art Unit 2817

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